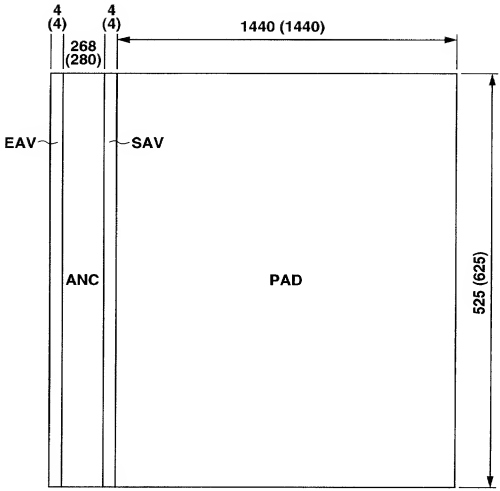


FIG.1

FIG.2A

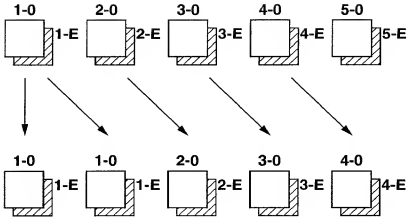
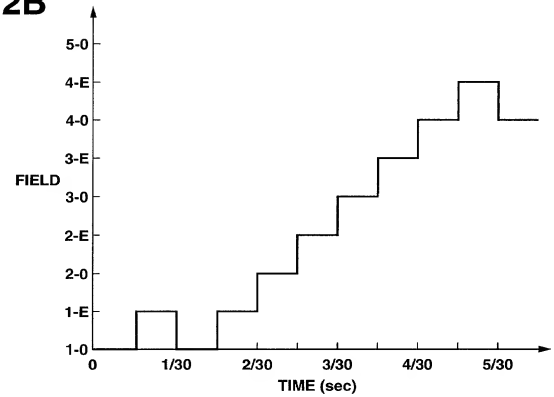


FIG.2B



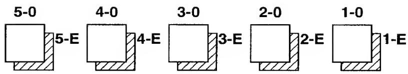

5-0
5-E
4-0
4-E
3-0
3-E
2-0
2-E
1-0
1-E

FIG.3A

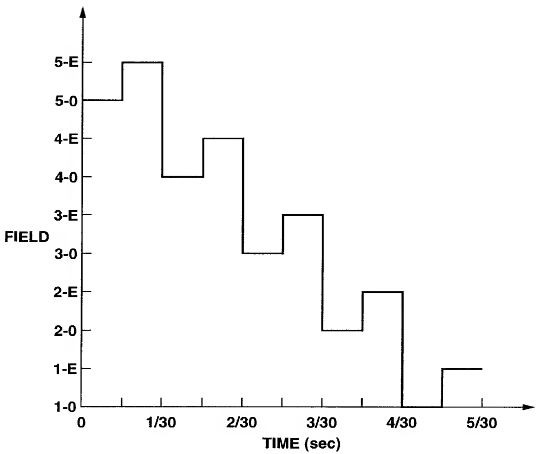

FIELD
5-E
5-0
4-E
4-0
3-E
3-0
2-E
2-0
1-E
1-0
0
1/30
2/30
3/30
4/30
5/30
TIME (sec)

FIG.3B

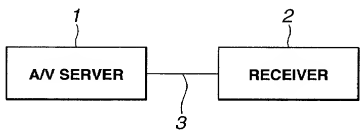


FIG.4

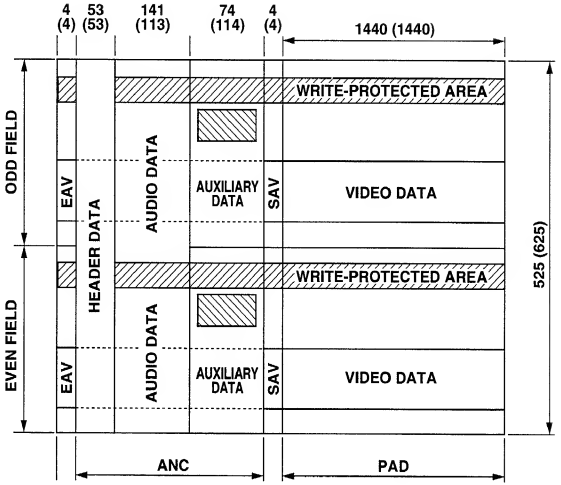


FIG.5

FIG.6

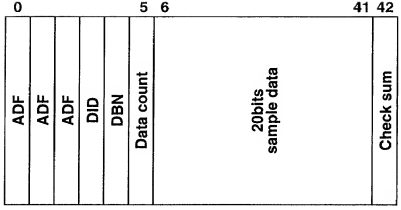


FIG.7A

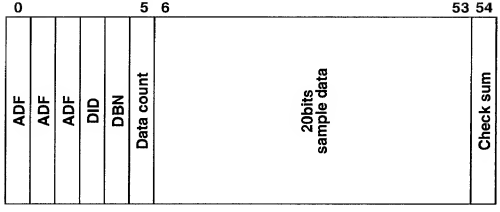


FIG.7B

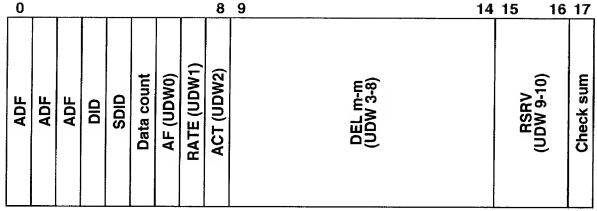


FIG.8

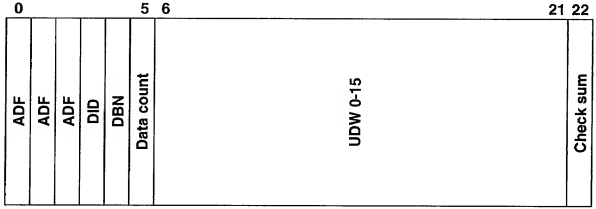


FIG.9

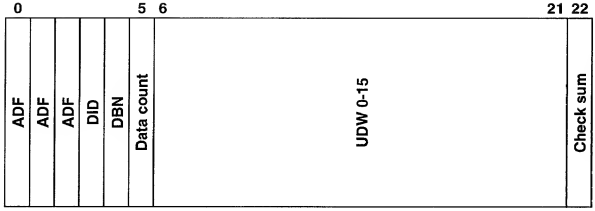


FIG.10

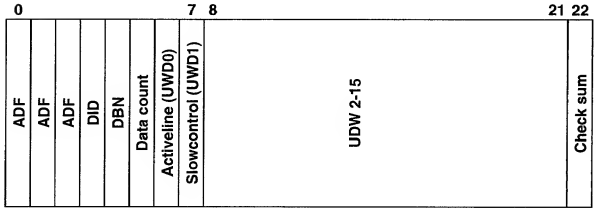


FIG.11

BIT	
7	Reserved
6	Reserved
5	Reserved
4	Contents information
3	Combination of the memory address
2	
1	
0	

FIG.12

FIG.13A

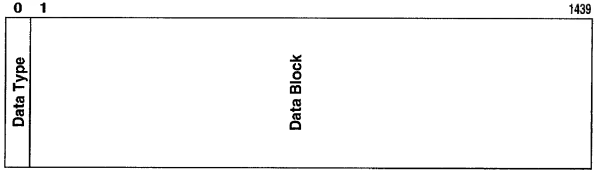
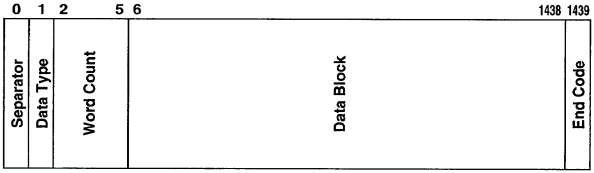


FIG.13B



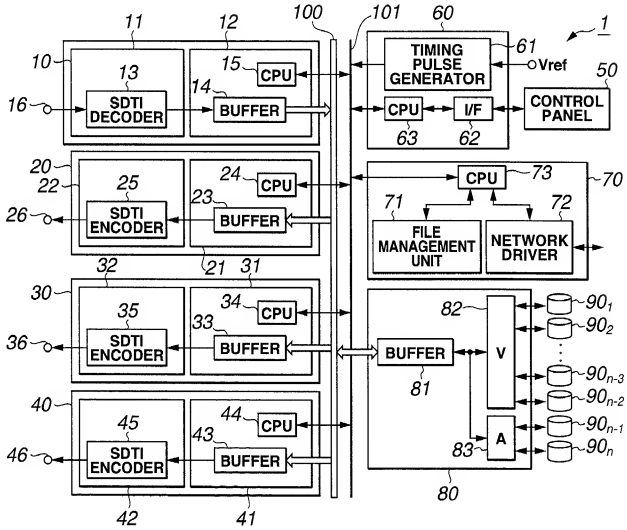

11
12
100
101
60
1
10
13
SDTI DECODER
15
CPU
14
BUFFER
16
TIMING PULSE GENERATOR
61
Vref
50
CONTROL PANEL
CPU
I/F
63
62
20
22
25
SDTI ENCODER
24
CPU
23
BUFFER
26
CPU
73
70
71
72
FILE MANAGEMENT UNIT
NETWORK DRIVER
32
21
31
30
35
SDTI ENCODER
34
CPU
33
BUFFER
36
82
BUFFER
81
V
A
83
90_1
90_2
90_{n-3}
90_{n-2}
90_{n-1}
90_n
80
40
45
SDTI ENCODER
44
CPU
43
BUFFER
46
42
41

FIG.14

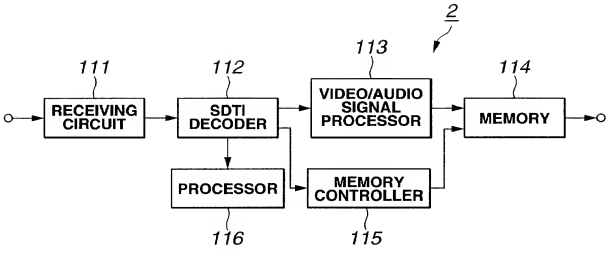


FIG.15

FIG.16A

FIG.16B

FIG.16C

FIG.17A

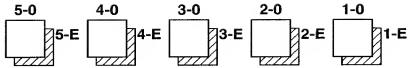


FIG.17B

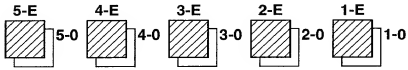


FIG.17C

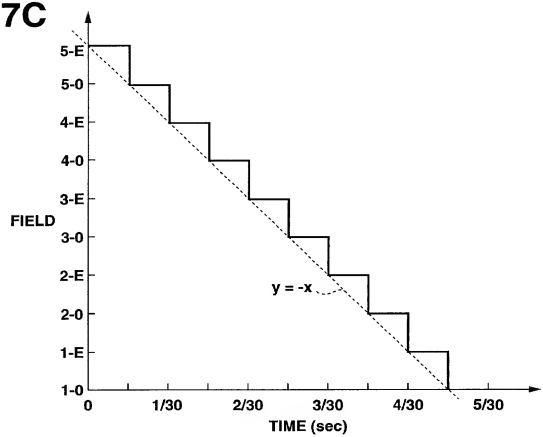


FIG.18A

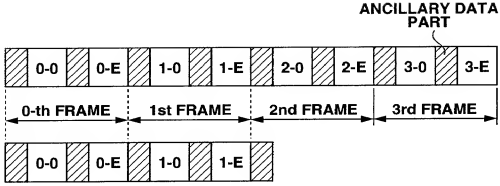


FIG.18B

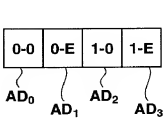


FIG.18C

FIG.18D

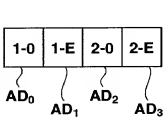


FIG.19A

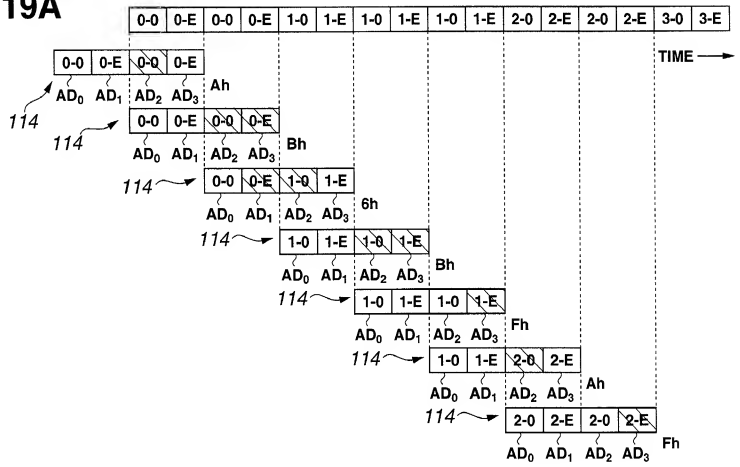


FIG.19B